

**REMARKS**

Upon entry of this amendment, claims 1-10 and 12-21 are all the claims pending in the application. Claim 21 has been added as a new claim. No new matter has been added.

**I. Claim Rejections under 35 U.S.C. § 103(a)**

A. Claims 1 and 10 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujinami et al. (U.S. 5,568,274) in view of Daum (U.S. 5,596,420).

Claim 1, as amended, recites the feature of a data formatter operable to output predetermined data in accordance with matching status information when the sequence of input code is judged not to be a part of the packet start code but to be a part of a particular sequence of coded data, and not to output predetermined data when the sequence of input code is judged to be a part of the packet start code, wherein the particular sequence of coded data and the packet start code have similar patterns. Applicants respectfully submit that Fujinami and Daum do not disclose or suggest the above-noted features recited in amended claim 1.

Regarding Fujinami, Applicants note that this reference discloses a separation circuit 21 which includes a header separation circuit 22, a switching circuit 23 and a control circuit 24 (see Fig. 12). The header separation circuit 22 separates the pack headers, packet headers and entry packets from a signal read out from the DSM 10 and supplies them to the control circuit 24 (see Fig. 12 and col. 15, lines 13-16). As disclosed in Fujinami, the remaining time-division multiplexed signal is supplied to the input terminal G of the switching circuit 23, and the control circuit 24 causes the switching circuit 23 to connect the input terminal G successively to output

terminals H1 and H2 in accordance with a stream ID of the packet header received from the header separation circuit 22 (see col. 15, lines 16-18 and 29-33).

Thus, in Fujinami, the packet headers are separated from the signal by the header separation circuit 22 and transferred to the control circuit 24, with the remaining portion of the signal being transmitted from the header separation circuit 22 to the switching circuit 23.

As noted above, claim 1 recites that the data formatter is operable to output predetermined data in accordance with matching status information when the sequence of input code is judged not to be a part of the packet start code but to be a part of a particular sequence of coded data, and not to output predetermined data when the sequence of input code is judged to be a part of the packet start code.

With respect to the above-noted features, based on the Examiner's comments on pages 3-4 of the Office Action, it appears as though the Examiner is taking the position that, in Fujinami, the video data and audio data output from the switching circuit 23 correspond to the claimed "predetermined data", that the signal output from the control circuit 24 corresponds to the claimed "matching status information", and that the switching circuit 23 corresponds to the claimed "data formatter".

Regarding the Examiner's position, Applicants note that, in Fujinami, while video data and audio data are output from the switching circuit 23 based on the signal that is received from the control circuit 24, that the switching circuit 23 does not operate so as output the video data and audio data in accordance with a signal received from the control circuit 24 when a sequence of input code is judged not to be a part of the packet start code but to be a part of a particular sequence of coded data. Instead, in Fujinami, it is merely disclosed that when a sequence of

input code is judged by the header separation circuit 22 to not be a part of the packet start code (e.g., the information other than the packet headers), that such information is transmitted from the header separation circuit 22 to the switching circuit 23.

Further, Applicants note that while Fujinami discloses that video data and audio data are output from the switching circuit 23 based on the signal that is received from the control circuit 24, that the switching circuit 23 does not operate so as to not output predetermined data when the sequence of input code is judged to be a part of the packet start code. In this regard, Applicants note that in the Office Action, the Examiner has indicated that because Fujinami discloses the conditions under which data is output, that this implicitly means that data is not output under different conditions (see page 2 of the Office Action).

With respect to such a position, Applicants note that the condition in Fujinami in which data is output is the receipt by the switching circuit 23 of a signal that is output from the control circuit 24. Thus, while Fujinami may implicitly disclose that when a signal is not received at the switching circuit 23 from the control circuit 24, that no data output will take place, Applicants respectfully submit that there is simply no disclosure (either explicit or implicit) in Fujinami suggesting that the switching circuit 23 does not output predetermined data when the sequence of input code is judged to be a part of the packet start code. Indeed, in Fujinami, when a packet header is output from the header separation circuit 22 to the control circuit 24, the result is that the control circuit 24 sends a signal to the switching circuit 23 informing the switching circuit 23 of the type of data that is to be output.

Based on the foregoing, Applicants respectfully submit that Fujinami does not disclose, suggest or otherwise render obvious at least the above-noted feature in amended claim 1 which

recites that the data formatter is operable to output predetermined data in accordance with matching status information when the sequence of input code is judged not to be a part of the packet start code but to be a part of a particular sequence of coded data, and not to output predetermined data when the sequence of input code is judged to be a part of the packet start code.

If the Examiner disagrees, and believes that Fujinami discloses such a feature, Applicants kindly request that the Examiner explicitly identify the elements in Fujinami that are being relied upon as corresponding to the claimed “data formatter”, the “predetermined data”, the “matching status information”, and the “sequence of input code”, so that Applicants can make an informed decision with regard to appeal.

Furthermore, as noted above, claim 1 has also been amended so as to recite that the particular sequence of coded data and the packet start code have similar patterns. Regarding such a feature, Applicants respectfully submit that, in Fujinami, the packet header and the audio/video data do not have similar patterns. As such, Applicants respectfully submit that Fujinami does not disclose or suggest the above-noted feature recited in claim 1.

In view of the foregoing, Applicants respectfully submit that Fujinami does not disclose, suggest or otherwise render obvious the above-noted feature recited in claim 1 of a data formatter operable to output predetermined data in accordance with matching status information when the sequence of input code is judged not to be a part of the packet start code but to be a part of a particular sequence of coded data, and not to output predetermined data when the sequence of input code is judged to be a part of the packet start code, wherein the particular sequence of

coded data and the packet start code have similar patterns. Further, Applicants respectfully submit that Daum does not cure this deficiency of Fujinami.

Accordingly, Applicants submit that claim 1 is patentable over the cited prior art, an indication of which is kindly requested. Claim 10 depends from claim 1 and is therefore considered patentable at least by virtue of its dependency.

B. Claims 5 and 15 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujinami et al. in view of Daum, and further in view of Toyohara (U.S. 5,768,265).

Claims 5 and 15 depend from claim 1. Applicants submit that Toyohara fails to cure the deficiencies of Fujinami et al. and Daum, as discussed above, with respect to claim 1.

Accordingly, Applicants submit that claims 5 and 15 are patentable at least by virtue of their dependency.

C. Claims 6, 7, 16 and 17 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Fujinami et al. in view of Daum and Toyohara, and further in view of Boden (U.S. 5,633,686).

Claims 6, 7, 16 and 17 ultimately depend from claim 1. Applicants submit that Boden fails to cure the deficiencies of Fujinami et al., Daum, and Toyohara, as discussed above, with respect to claim 1. Accordingly, Applicants submit that claims 6, 7, 16 and 17 are patentable at least by virtue of their dependency.

D. Claims 8, 9 and 18 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Yanagihara et al. (U.S. 6,172,989) in view Fujinami et al. (US 5,568,274), and further in view of Movshovich et al. (U.S. 6,359,911).

Claim 8, as amended, recites the feature of a formatter operable to pad a data bus with a predetermined number of pseudo data so that the code sequence indicating the end of the coded data is forwarded to the next stage of pipeline, when a code sequence indicating the end of the coded data is detected by said end code sequence detector. Applicants submit that the combination of Yanagihara, Fujinami, and Movshovich does not teach or suggest at least this feature of claim 8.

Regarding Yanagihara, Applicants note that it is disclosed therein that in order to transmit data in accordance with IEEE 1394, a pack forming a unit of MPEG-PS data (which has a length of 2,048 bytes) can be converted into packets that are transmitted in accordance with IEEE 1394 (see col. 3, lines 5-12). In order to convert the MPEG-PS data into a packet that is transmitted in accordance with the IEEE 1394 standard, padding data is added.

For example, in the Abstract of Yanagihara and in col. 7, lines 1-7, it is disclosed that Yanagihara is able to add padding data to a 2,048 byte pack of MPEG-PS data so that the overall byte length of data is a multiple of 16. Thus, in Yanagihara the padding data is added so that data packets can be divided into data blocks having a size (e.g., 36 byte data blocks as shown in Fig. 16(E)) that is necessary to convert the MPEG-PS data pack into packets that conform with IEEE 1394.

As noted above, claim 8 now recites the feature of a formatter that is operable to pad a data bus with a predetermined number of pseudo data so that the code sequence indicating the

end of the coded data is forwarded to the next stage of pipeline. Applicants respectfully submit that Yanagihara clearly does not disclose or suggest such a feature.

Further, regarding Fujinami and Movshovich, Applicants note that while Fujinami discloses the ability to selectively control the output of audio/video data, and Movshovich discloses the use of pipeline transfer, that neither reference, either alone or in combination with Yanagihara, renders obvious the above-noted feature recited in amended claim 8 of a formatter that is operable to pad a data bus with a predetermined number of pseudo data so that the code sequence indicating the end of the coded data is forwarded to the next stage of pipeline.

Accordingly, Applicants submit that amended claim 8 is patentable over the cited prior art, an indication of which is kindly requested. Claims 9 and 18 depend from claim 8 and are therefore considered patentable at least by virtue of their dependency.

## **II. Allowable Subject Matter**

Applicants thank the Examiner for indicating that claims 2-4 and 12-14 contain allowable subject matter and would be allowable if rewritten in independent form.

## **III. New Claims**

Claim 21 has been added as a new claim. Claim 21 depends from claim 1 and is therefore considered patentable at least by virtue of its dependency.

## **IV. Conclusion**

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited.

If any points remain in issue, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Respectfully submitted,

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